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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 49 (A8)

Application Number: 08/901,338
Filing Date: July 28, 1997
Appellant(s): KEESMAN, GERRIT J.

Cherie S. Werbel (#40,870)
For Appellant

EXAMINER'S ANSWER

This is in response to Appellant Brief on appeal filed on 4/03/01 as Paper 48.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

A statement is present that the claims stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,561,466	Kiriyama	10-1996

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-12 and 14 are currently rejected under 35 U.S.C. 102(e) as being anticipated by Kiriyama. This rejection is set forth in prior Office Action mailed on 5/16/00 as Paper # 42, and maintained in the final Office Action mailed on 11/01/00 as Paper #44. However, it is noted that in the detailed Office Actions, the Examiner has mistakenly referred to the reference as "Kirayama" and not as the correctly spelled "Kiriyama" as the patentee's name appears on the reference. The Examiner apologizes for any confusion caused by this inadvertent typographical error.

(11) Response to Argument

Applicant's arguments filed in the Appeal Brief of Paper 48 on 4/03/01 have been fully considered but they are not persuasive. The Appellant presents two substantive arguments

contending the Examiner's rejection of claims 1-12 and 14 under 35 U.S.C. 102(e) as being anticipated by Kiriyama, as was forth in prior Office Action mailed on 5/16/00 as Paper # 42, and maintained in the final Office Action mailed on 11/01/00 as Paper #44. However, after a careful consideration of the arguments presented, the Examiner must respectfully disagree, submit to the Board that the rejection should be sustained.

Firstly, after summarizing the Examiner's application of the Kiriyama reference (Paper 48: page 3, lines 7-22; page 4, lines 1-17), the Appellant asserts that Kiriyama does not establish an inverse relationship between the encoder buffer input rate (B1) and the bit-rate of the data stream leaving the decoder buffer (B2), but argues that the respective buffer rates are equal (Paper 48: page 4, lines 18-24; page 1-7). The Examiner respectfully disagrees. In particular, the Examiner notes that the delay associated with the encoder buffer input rate (B1) is actually transmitted (Kiriyama: column 6, lines 35-61) to the decoder buffer (Kiriyama: column 9, lines 35-60) which establishes that the decoder buffer is aware of the data rates associated with the encoder buffer throughput. Further, Kiriyama states that this sum delay in the bit transfer rate through the encoder buffer memory (Kiriyama: figure 5, element 39) plus the additional video delay becomes equal to a predetermined video delay THV (Kiriyama: column 10, lines 16-19). The sum delay in the bit transfer rate through the encoder buffer memory has to be equal to the delay associated with the output bit rate of the encoder plus the delay associated with encoder buffer input rate (B1), since one cannot assume a constant delay with the encoder buffer memory being controlled by the buffer read controller (Kiriyama: column 8, lines 34-50). Additionally, it's not the data rate of the stream leaving the decoder buffer (B2) that is relevant to the claims, but rather the data rate of the stream entering the decoder buffer (B3) that is of interest. A

mathematical explanation would best illustrate the point of establishing an inverse relationship. If we call the delay associated with the output bit rate of the encoder buffer (B0), then the sum delay of the delay of the encoder buffer memory is show by the following equation:

(1) Sum Delay of encoder buffer memory = (B0) + (B1)

Now this Sum Delay of plus some "additional video delay" becomes equal to predetermined video delay THV (Kiriyama: column 10, lines 16-19). Now the "additional video delay" is a broad term, but if we take Appellant's assertion in a subsequent argument that this additional video delay is actually the delay associated with decoder buffer (Paper 48: page 7, lines 1-15), then this additional video cannot just be the delay associated with the decoder buffer's output bit rate (B2), but must be also considered in terms of a bit transfer rate associated with the decoder buffer including some mention of the delay associated with the input bit-rate to the decoder buffer (B3), computed in terms of a decoder buffer occupancy signal (Kiriyama: column 14, lines 50-55). Again an equation illustrates the behavior the decoder buffer (Kiriyama: figure 7, element 71)

(2) Sum Delay of the decoder buffer delay = (B2) + (B3)

Kiriyama further clarifies the use of THV with the "sum delay" of the reference (Kiriyama: column 10, lines 16-19), and actually notes that "sum delay" is the sum delay of the encoder buffer delay plus the sum delay of the decoder buffer delay (Kiriyama: column 14, lines 55-65),

and thus the manipulation of the THV predetermined video delay can be represented by the following equation:

(3) [((B1) + (B0)) + ((B2) + (B3))] + "additional video delay" = THV

where

B0 = delay associated with the encoder buffer input rate

B1 = delay associated with the encoder buffer output rate

B2 = delay associated with the decoder buffer output rate

B3 = delay associated with the decoder buffer input rate

Clearly what this establishes is that the "additional video delay" is not associated with the decoder buffer read out delay as asserted by the Appellant's subsequent argument (Paper 48: page 7, lines 1-15), but that this "additional video delay" is actually the propagation delay of transmission. That's why Kiriyama makes a statement about now being able to determine the propagation delay of the multiplexer device (Kiriyama: column 10, lines 23-25). Additionally, what this also establishes is that the respective buffer rates are not equal as argued by the Appellant (Paper 48: page 4, lines 18-24; page 1-7), but rather a counterbalancing set of variables. Now, we go back to the equation of interest:

(4) [((B1) + (B0)) + ((B2) + (B3))] = THV -"additional video delay"

An approximation can be made that the output rate of the encoder buffer should equal the input rate of the decoder buffer, because one is assuming that no bits will be lost during transmission. Of course in actual practice, bits are lost and error correction on the decoder side has to occur to overcome problems in transmission, but ideally, B1 equals B3. This makes the equation much simpler to handle:

(4) [((B0) + (B2)) + 2(B3))] = THV -"additional video delay"

Isolating B0 and B3 on opposite sides of the above equation, and abbreviating for "additional video delay" yields:

(5) **(B0) = -2(B3) + [(THV) - (B2) – (ADV)]**

This final equation relates the B0 in terms of B3, where B0 is delay associated with the encoder buffer input rate, and B3 is delay associated with the decoder buffer input rate. This final equation is in the well recognizable form of a standard linear algebraic equation of y = mx + b with the equation's terms corresponding to the following:

Y = (B0)

X = (B3)

M = -2

B = [(THV) - (B2) – (ADV)]

The fact that the slope of the –2 defines the mathematical equation (5) as an inverse relationship because of the negative slope and clearly contradicts the Appellant's position that no relationship exists between the encoder buffer input rate and the decoder buffer input rate (Paper 48: page 5, lines 1-7). Additionally, while the Appellant reinforces the point about Kiriyama being directed towards a different problem (Paper 48: page 5, lines 8-25), it is noted that one of Kiriyama's controlling conditions for the decoder buffer is such that overflow and underflow conditions are monitored and accounted for (Kiriyama: column 10, lines 9-15), so the Examiner would further offer that while lip synchronism is to be achieved, it is not at the expense of the reference's required buffer control, and the Examiner further offers that those two teachings are not contradictory. Also, the Appellant further goes onto mention that (B2) as in the instant invention is totally different from the decoder buffer read-out rate and the delay associated therewith (Paper 48: page 6, lines 3-15). The Examiner agrees, however, as was discussed above, the decoder buffer read-in rate or input rate is what is relevant and has been shown to have the relationship as required by the claims.

After outlining the quotation of text in question (Paper 48: page 7, lines 4-15), and accurately paraphrasing the Examiner's stance in the previous Office Action (Paper 48: page 7, lines 16-21; page 8, lines 1-8), the Appellant additionally argues that the Examiner's argument is flawed and interpreted out of context (Paper 48: page 6, lines 16-26; page 7, lines 1-4). The Examiner respectfully disagrees. Both sides seem to agree that the reference's citation establishes that this sum delay of the encoder buffer plus some "additional video delay" becomes equal to a predetermined video delay THV (Kiriyama: column 10, lines 16-19). Now,

"additional video delay" is a broad term, but if we take Appellant's assertion in a subsequent argument that this additional video delay is actually the delay associated with decoder buffer (Paper 48: page 7, lines 1-15), then this additional video cannot just be the delay associated with the decoder buffer's output bit rate (B2), but must be also considered in terms of a bit transfer rate associated with the decoder buffer including some mention of the delay associated with the input bit-rate to the decoder buffer (B3), computed in terms of a decoder buffer occupancy signal (Kiriyama: column 14, lines 50-55; figure 7, element 71). This point is more important to the mathematical explanation of the first argument. However, Kiriyama further clarifies the use of THV with the "sum delay" of the reference (Kiriyama: column 10, lines 16-19), and actually notes that the "sum delay" is the sum delay of the encoder buffer delay plus the sum delay of the decoder buffer delay (Kiriyama: column 14, lines 55-65), and thus the manipulation of the THV predetermined video delay can be represented by the following equation:

$$(3)\ Delay_E + Delay_D + \text{"additional video delay"} = THV$$

where

$Delay_E$ = sum delay associated with the encoder buffer

$Delay_D$ = sum delay associated with the decoder buffer

Clearly what this establishes is that the "additional video delay" is not associated with the decoder buffer read out delay as asserted by the Appellant's subsequent argument (Paper 48: page 7, lines 1-15; page 8, lines 1-8), but that this "additional video delay" is actually the propagation delay of transmission. Basis for this from the reference can be found by Kiriyama's

statement about now being able to determine the propagation delay of the multiplexer device (Kiriyama: column 10, lines 23-25). Appellant's interpretation of the "...from the video buffer memory..." respectfully considered by the Examiner to be completely erroneous (Paper 48: page 8, lines 9-20). If that were the case then there would be there would be some sort of feed back from the decoder to the decoder buffer read-out controller controlling the read-out process. Looking at figure 8, we see that this is not the case. Furthermore, it is noted that the correct citation (Kiriyama: column 9, lines 58-61) is the following:

> "...From the video buffer memory **71**, the read video data read with *an additional video delay relative to the production of the separated video data from the video processor* **65**..."

The additional video delay is localized by the reference as being relative to the production of the separated video from the video processor (Kiriyama: figure 8, element 65), and is an element in the codec chain ahead of the buffer. Additionally, the reference states that the read video data re produced from the video buffer memory with the sum delay relative to the supply of the encoded video signal to the encoder buffer memory (Kiriyama: column 10, lines 20-25; figure 5, element 39). Accordingly, without a feedback signal to the decoder video buffer read out controller (Kiriyama: figure 8, element 75) from the decoder, and the statement that the video buffer is producing data relative to the supply of the encoded data to the buffer memory, means that this "additional video delay" is looking at the codec chain. The comments concerning the Appellant encoder buffer readout rate and the inverse relationship (Paper 48: page 8, lines 21-25; page 9, lines 1-8) have been more completely dealt with above and will not be repeated here.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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